

MH285 is an unipolar Hall effect sensor IC. It incorporates advanced chopper Stabilization technology to provide accurate and stable magnetic switch points. The desigh, specifications and performance have been optimized for applications of solid state switches.

The output transistor will be switched on  $(B_{OP})$  in the presence of a sufficiently strong South pole magnetic field facing the marked side of the package. Similarly, the output will be switched off  $(B_{RP})$  in the presence of a weaker South field and remain off with "0" field.

The package type is in a Halogen Free version was verified by third party organization. Halogen Free package is available by customer's option.

#### Features and Benefits

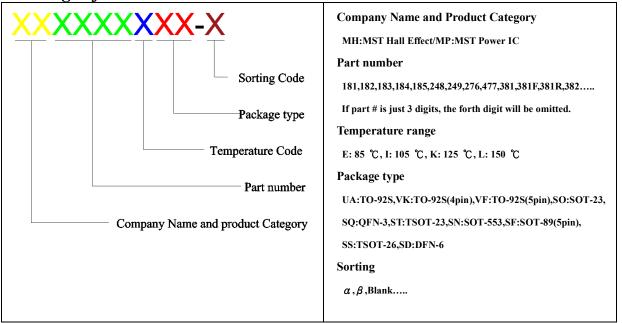
- DMOS Hall IC Technology
- Reverse bias protection on power supply pin
- Good ESD protection
- Solid-State Reliability
- Chopper stabilized amplifier stage
- Unipolar, output switches with absolute value of South pole from magnet
- Operation down to 2.5v
- High sensitivitiy direct reed switch replacement applications
- 100% tested at 125°C for K spec
- Custom sensitivity/Temperature selection are availabe.
- RoHS compliant 2011/65/EU and Halogen Free.

### **Applications**

- Solid state switch
- Limit switch.
- Current limit
- Interrupter
- Current sensing
- Magnet proximity sensor for reed switch replacement



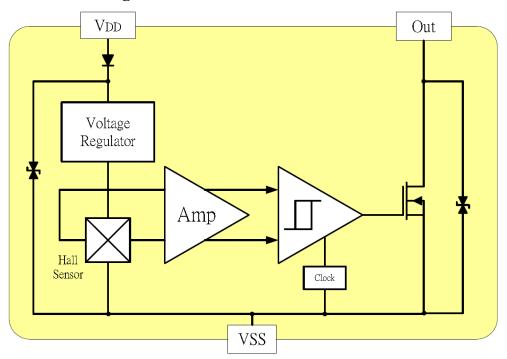
**Ordering Information** 



Part No.	Temperature Suffix	Package Type	
MH285KUA	$K (-40^{\circ}C \text{ to} + 125^{\circ}C)$	UA (TO-92S)	
MH285EUA	E $(-40^{\circ}\text{C to} + 85^{\circ}\text{C})$	UA (TO-92S)	
MH285KSO	$E (-40^{\circ}C \text{ to} + 125^{\circ}C)$	SO (SOT-23)	

Custom sensitivity selection is available by MST sorting technology

## Functional Diagram



Note: Static sensitive device; please observe ESD precautions. Reverse  $V_{DD}$  protection is not included. For reverse voltage protection, a  $100\Omega$  resistor in series with  $V_{DD}$  is recommended.



Absolute Maximum Ratings At (Ta=25°C)

Characteristics			Values	Unit
Supply voltage,(VDD)			28	V
Output Voltage,(Vout)			28	V
Reverse voltage, (VDD) (VOUT)			-27/-0.3	V
Magnetic flux density			Unlimited	Gauss
Output current,( <i>I<sub>SINK</sub></i> )			50	mA
On anotin a Tanan anatuma Ram	, (Ta)	"E" version	-40 to +85	°C
Operating Temperature Ran	ige, (1a)	"K" version	-40 to +125	°C
Storage temperature range, ( <i>Ts</i> )			-55 to +150	°C
Maximum Junction Temp, $(Tj)$			150	°C
Thermal Resistance	$(\theta JA) \text{ UA / SO}$		206 / 543	°C/W
	(θJC) UA / SO		148 / 410	°C/W
Package Power Dissipation, (PD) UA / SO			606 / 230	mW

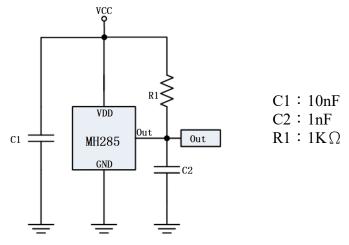
**Note:** Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

# **Electrical Specifications**

DC Operating Parameters TA=+25°C, VDD=12V

Parameters	<b>Test Conditions</b>	Min	Тур	Max	Units
Supply Voltage,(VDD)	Operating	2.5		24.0	V
Supply Current,( <i>I</i> <sub>DD</sub> )	B <bop< td=""><td></td><td>2.5</td><td>5.0</td><td>mA</td></bop<>		2.5	5.0	mA
Output Low Voltage,(VDSON)	IOUT=20mA, B>Bop			500	mV
Output Leakage Current,(Ioff)	IOFF B <brp, vout="20V&lt;/td"><td></td><td></td><td>10.0</td><td>uA</td></brp,>			10.0	uA
Power-On Time, ( <i>Tp</i> )				50	uS
Output Switch Time, (Tsw )				150	uS
Output Switch Frequency,(Fsw)		3			KHz
Out put Rise Time, $(T_R)$	$R_L=1K\Omega; C_L=20_PF$		0.04	1.0	uS
Out put Fall Time, (T <sub>F</sub> )	$R_L=1K\Omega; C_L=20_PF$		0.18	1.0	uS
Electro-Static Discharge	HBM	4			KV
Operate Point, (B <sub>OP</sub> )	UA(SO)	15(-35)		35(-15)	Gauss
Release Point,(B <sub>RP</sub> )	UA(SO)	7(-27)		27(-7)	Gauss
Hysteresis,(Bhys)	Bop - Brp		8		Gauss

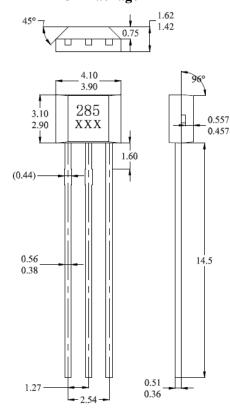
## Typical Application circuit



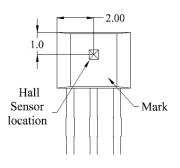


### Sensor Location, Package Dimension and Marking

#### **UA Package**

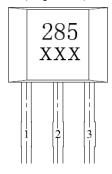


#### **Hall Chip location**



#### **Output Pin Assignment**

#### (Top view)



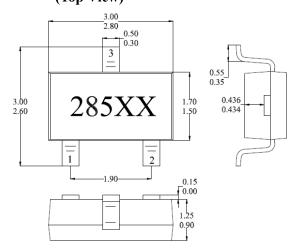
#### **NOTES:**

- 1).Controlling dimension: mm
- 2).Leads must be free of flash and plating voids
- 3).Do not bend leads within 1 mm of lead to package interface.
- 4).PINOUT:

Pin 1 VDD Pin 2 GND Pin 3 Output

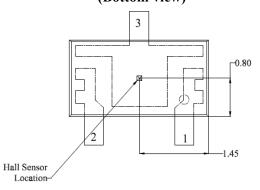
### **SO Package**

#### (Top View)



#### **Hall Plate Chip Location**

#### (Bottom view)



### (For reference only)Land Pattern

#### **NOTES:**

- 1. PINOUT (See Top View at left :)
  - Pin 1 V<sub>DD</sub>
  - Pin 2 Output
  - Pin 3 GND
- 2. Controlling dimension: mm
- 3. Lead thickness after solder plating will be 0.254mm maximum

