

MH178 Hall-effect latch is a temperature stable, stress-resistant, mini-power IC. Superior high-temperature performance is made possible through a dynamic offset cancellation that utilizes chopper-stabilization. This method reduces the offset voltage normally caused by device over molding, temperature dependencies, and thermal stress.

MH178 includes the following on a single silicon chip: voltage regulator, Hall voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, open-drain output. Advanced CMOS wafer fabrication processing is used to take advantage of low-voltage requirements, component matching, very low input-offset errors, and small component geometries.

This device requires the presence of both south and north polarity magnetic fields for operation. In the presence of a south polarity field of sufficient strength, the device output sensor on, and only switches off when a north polarity field of sufficient strength is present.

MH178 is rated for operation between the ambient temperatures  $-40^{\circ}\text{C}$  and  $+85^{\circ}\text{C}$ , and  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  for the K temperature range. for the E temperature range. The two package styles available provide magnetically optimized solutions for most applications. Package SO is an SOT-23, a miniature low-profile surface-mount package, while package UA is a three-lead ultra mini SIP-3 for through-hole mounting.

The package type is in a lead Halogen Free version was verified by third party Lab.

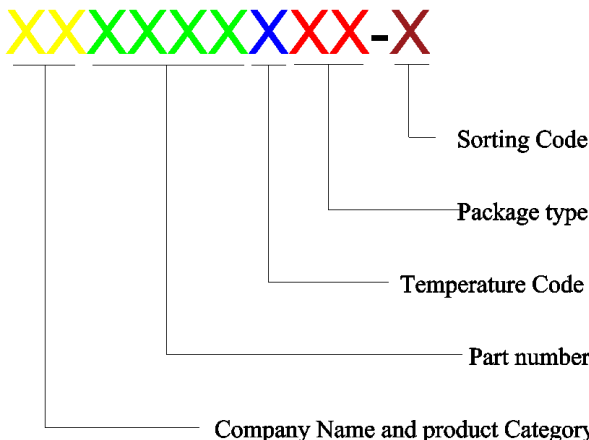
### ***Features and Benefits***

- CMOS Hall IC Technology
- Strong RF noise protection
- 2.0 to 5.5V for battery-powered applications
- Operation down to 2.0V, Micro power consumption
- 100% tested at  $125^{\circ}\text{C}$  for K
- Low sensitivity drift in crossing of Temp range
- Ultra Low power consumption at  $9\mu\text{A}$  (Avg)
- High ESD Protection, HBM  $> \pm 4\text{KV}$ ( min )
- Open Drain output
- RoHS compliant 2011/65/EU and Halogen Free

### ***Applications***

- Speed sensing
- Position sensing
- Revolution counting
- Solid-State Switch
- Current sensing
- Revolution counting
- Solid-State Switch

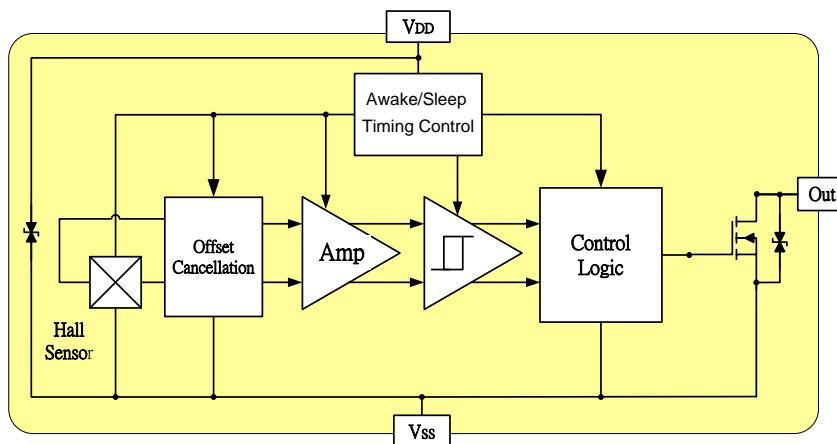
### Ordering Information

	<p><b>Company Name and Product Category</b> MH:MST Hall Effect/MP:MST Power IC</p> <p><b>Part number</b> 181,182,183,184,185,248,249,276,477,381,381F,381R,382..... If part # is just 3 digits, the forth digit will be omitted.</p> <p><b>Temperature range</b> E: 85 °C, I: 105 °C, K: 125 °C, L: 150 °C</p> <p><b>Package type</b> UA:TO-92S,VK:TO-92S(4pin),VF:TO-92S(5pin),SO:SOT-23, SQ:QFN-3,ST:TSOT-23,SN:SOT-553,SF:SOT-89(5pin), SS:TSOT-26,SD:DFN-6,SG:SOT-89(3pin)</p> <p><b>Sorting</b> <math>\alpha</math>, <math>\beta</math>, Blank.....</p>
---	--

Part No.	Temperature Suffix	Package Type
MH178KUA	K (-40°C to + 125°C)	UA (TO-92S)
MH178EUA	E (-40°C to + 85°C)	UA (TO-92S)
MH178ESO	E (-40°C to + 85°C)	SO (SOT-23)

Custom sensitivity selection is available by MST sorting technology

### Functional Diagram



**Note:** Static sensitive device; please observe ESD precautions. Reverse  $V_{DD}$  protection is not included. For reverse voltage protection, a  $100\Omega$  resistor in series with  $V_{DD}$  is recommended.



## MH178 Specifications Micropower Hall Effect Latch

### Absolute Maximum Ratings At ( $T_a=25^\circ\text{C}$ )

Characteristics		Values	Unit
Supply voltage, ( $V_{DD}$ )		6	V
Output Voltage, ( $V_{out}$ )		6	V
Reverse voltage, ( $V_{DD}$ ) ( $V_{out}$ )		-0.3	V
Magnetic flux density		Unlimited	Gauss
Output current, ( $I_{out}$ )		10	mA
Operating Temperature Range, ( $T_a$ )	“E” version	-40 to +85	$^\circ\text{C}$
	“K” version	-40 to +125	$^\circ\text{C}$
Storage temperature range, ( $T_s$ )		-65 to +150	$^\circ\text{C}$
Maximum Junction Temp, ( $T_j$ )		150	$^\circ\text{C}$
Thermal Resistance	( $\theta_{JA}$ ) UA / SO	206 / 543	$^\circ\text{C}/\text{W}$
	( $\theta_{JC}$ ) UA / SO	148 / 410	$^\circ\text{C}/\text{W}$
Package Power Dissipation, ( $P_D$ ) UA / SO		606 / 230	mW

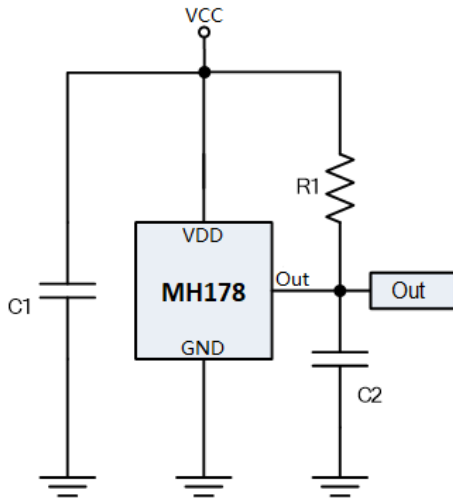
*Note: Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.*

### Electrical Specifications

DC Operating Parameters  $T_A=+25^\circ\text{C}$ ,  $V_{DD}=3.0\text{V}$

Parameters	Test Conditions	Min	Typ	Max	Units
Supply Voltage, ( $V_{DD}$ )	Operating	2.0		5.5	V
Supply Current, ( $I_{DD}$ )	Awake State		2.0	5.0	mA
	Sleep State		7.0	10.0	$\mu\text{A}$
	Average		9.0	15.0	$\mu\text{A}$
Output Saturation Voltage,	$I_{out}=5\text{mA}, B > BOP$			200	mV
Output Leakage Current, ( $I_{off}$ )	IOFF B < BRP, $V_{OUT} = 5.5\text{V}$			1.0	$\mu\text{A}$
Awake mode time, ( $T_{aw}$ )	Operating		40	80	$\mu\text{s}$
Sleep mode time, ( $T_{SL}$ )	Operating		40	80	mS
Duty Cycle, ( $D, C$ )			0.1		%
Response Time, ( $T_{RES}$ )				5	Hz
Output Rise Time, ( $T_R$ )	$R_L=1\text{K}\Omega, C_L=20\text{pF}$		0.18	0.45	$\mu\text{s}$
Output Fall Time, ( $T_F$ )	$R_L=1\text{K}\Omega; C_L=20\text{pF}$		0.18	0.45	$\mu\text{s}$
Electro-Static Discharge	HBM	4			KV
Operating Point ( $B_{OP}$ )	S pole to branded side, $B > BOP$ , $V_{out}$ On	5		40	Gauss
Release Point ( $B_{RP}$ )	N pole to branded side, $B < BRP$ , $V_{out}$	-40		-5	Gauss
Hysteresis ( $B_{HYS}$ )	$ BOP - BRP $		40		Gauss

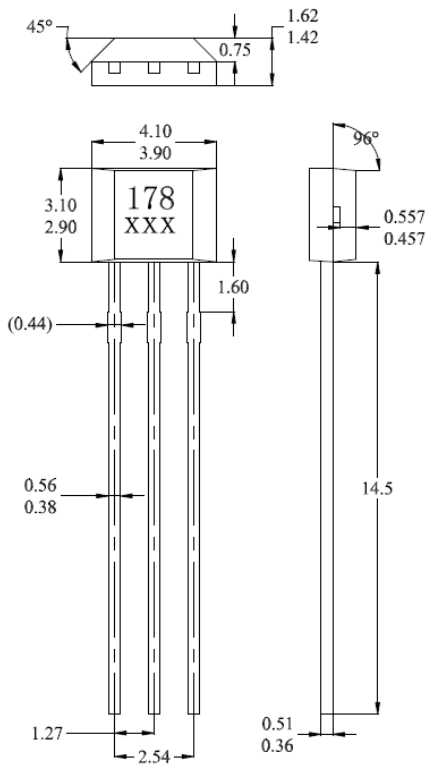
**Typical Application circuit**



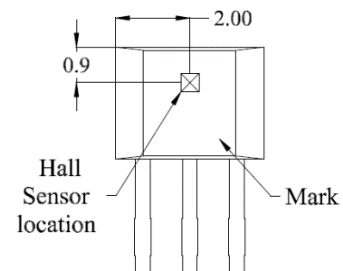
**C1 : 10nF**  
**C2 : 100pF**  
**R1 : 100KΩ**

**Sensor Location, Package Dimension and Marking**

**UA Package**



**Hall Chip location**



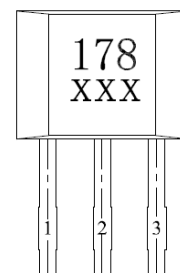
**NOTES:**

1. Controlling dimension: mm
2. Leads must be free of flash and plating voids
3. Do not bend leads within 1 mm of lead to package interface.

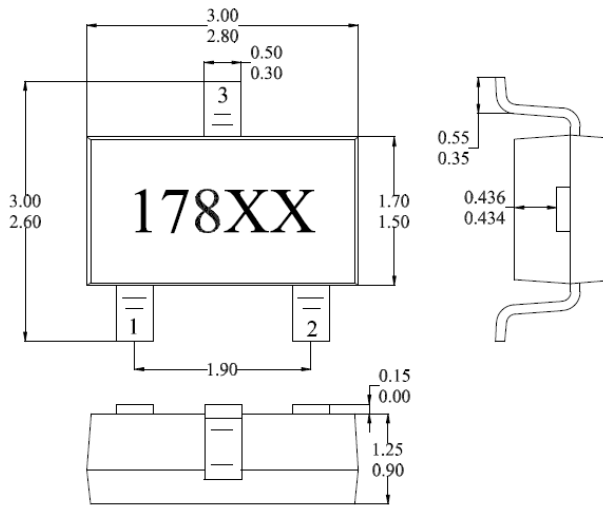
**4. PINOUT:**

Pin 1	VDD
Pin 2	GND
Pin 3	Output

**Output Pin Assignment**  
**(Top view)**



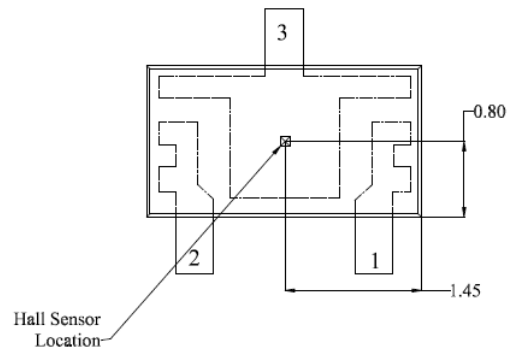
### SO Package (Top View)



### NOTES:

1. PINOUT (See Top View at left :)
  - Pin 1  $V_{DD}$
  - Pin 2 Output
  - Pin 3 GND
2. Controlling dimension: mm
3. Lead thickness after solder plating will be 0.254mm maximum

### Hall Plate Chip Location (Bottom view)



### (For reference only) Land Pattern

