The device is a magnetic field sensor for accurate measurements in harsh environments. It combines an integrated Hall-effect sensor with on-chip signal conditioning electronics to achieve an unsurpassed accuracy and dynamic range.

In a CMOS integrated Hall IC sensitivity varies with processing parameters of silicon. For an accurate sensitivity this parameter needs to be trimmed and coarse and fine trim bits are available. The temperature coefficient of the sensitivity needs to be trimmed as well to achieve 200ppm/°C

The on-chip memory is EEPROM that allows up to 1,000 write/erase cycles at factory trimming or in a customer application. Programming can be done using a normal 5V supply; high programming voltage is generated on-chip.

Features and Benefits

- Fully integrated Hall-effect based Magnetic Field sensor
- No internal magnetic circuit： no memory or saturation
- No user offset trimming required
- User-trimmable sensitivity and sensitivity temperature coefficient
- User-selectable internal or external reference voltage
- Fast response time
- RoHS compliant 2011/65/EU and Halogen Free

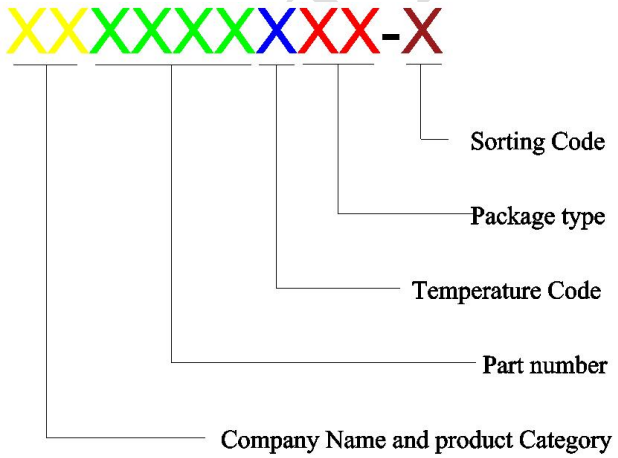
Applications

- Contactless ac/dc current monitoring
- Precise position sensing
- Magnetic field measurement
- Rotation detection

Application domains

- Industrial and consumer products

Ordering Information



Company Name and Product Category

MH:MST Hall Effect/MP:MST Power IC

Part number

181,182,183,184,185,248,249,276,477,381,381F,381R,382…..

If part # is just 3 digits, the forth digit will be omitted.

Temperature range

E: 85 ℃, I: 105 ℃, K: 125 ℃, L: 150 ℃

Package type

UA:TO-92S,VK:TO-92S(4pin),VF:TO-92S(5pin),SO:SOT-23,

SQ:QFN-3,ST:TSOT-23,SN:SOT-553,SF:SOT-89(5pin),

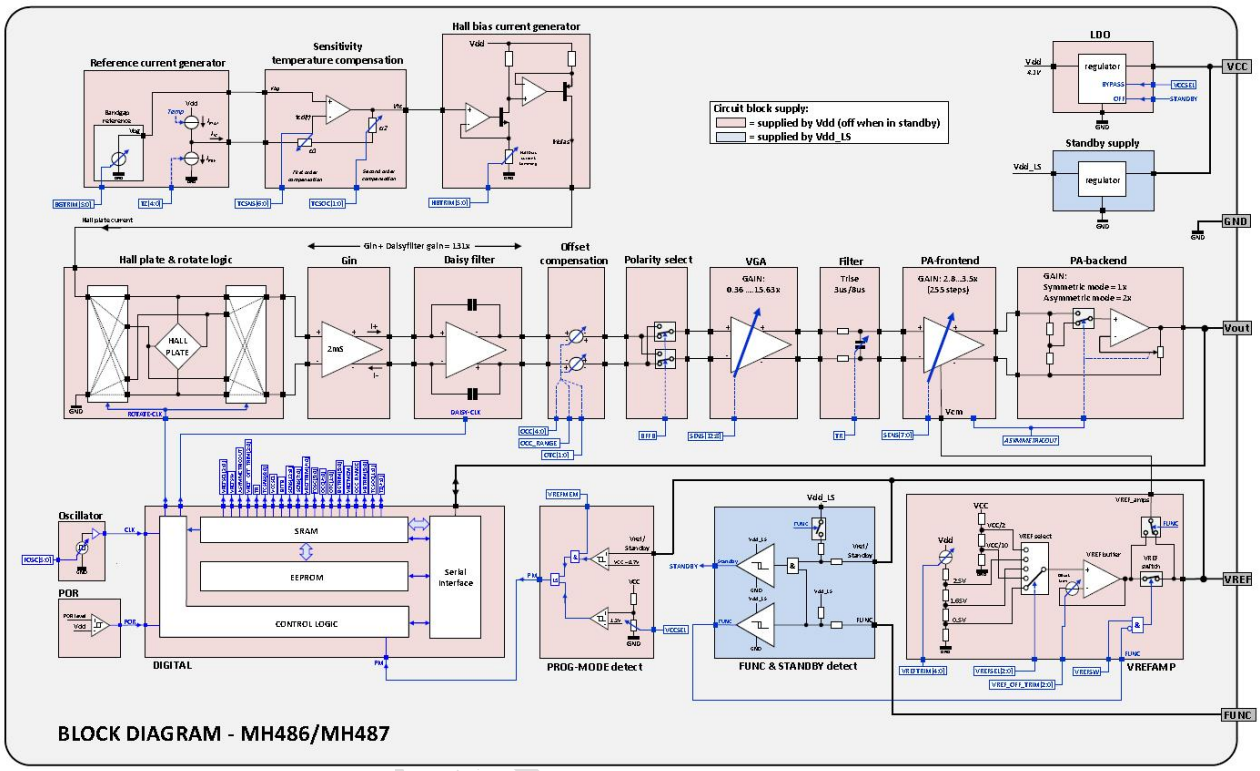
SS:TSOT-26,SD:DFN-6

Sorting

α,β,Blank…..

Part No.	Temperature Suffix	Package Type
MH485IVL	I (-40℃ to + 105℃)	VL (TO-94 3PIN)
MH486IVK	I (-40℃ to + 105℃)	VK (TO-94 4PIN)
MH487IVK	I (-40℃ to + 105℃)	VK (TO-94 4PIN)

Block Diagram



Absolute Maximum Ratings

PARAMETER	Min	Typ	Max	Unit
Junction temperature(T_J)	-55		165	°C
Supply voltage(normal operation)	-0.3		4.6[d]/6.5[e]	V

Operation outside these conditions can lead to immediate failure. Prolonged use of the device under these conditions may cause accelerated aging and early device failure.

Reverse Supply Protection

An ESD protection diode protects the circuit against negative voltage supplies that can occur if the battery/supply connection is inverted, as displayed in Figure 1. A maximum current of 50mA can be handled in the IC, therefore a current limitation has to be added in series with the supply to avoid any damages on the circuit, if over current occurs.

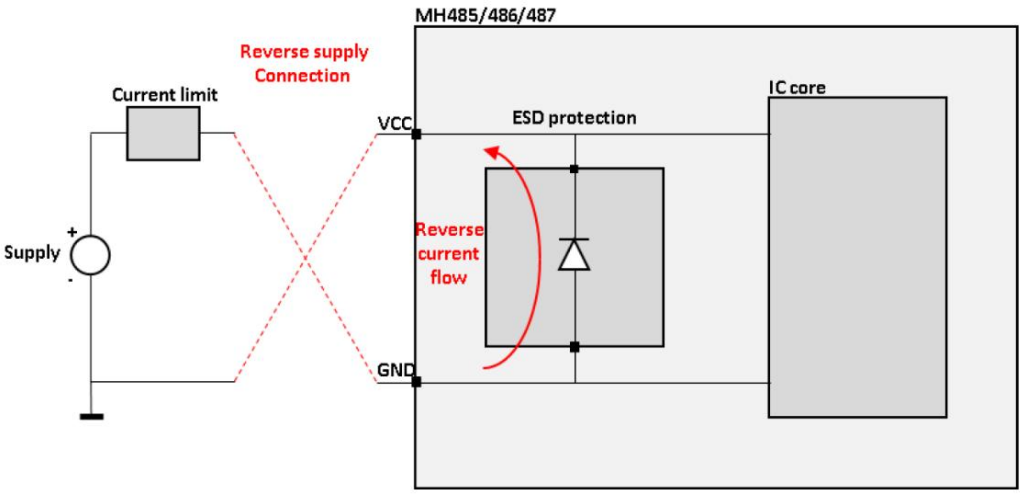


Figure 1: ESD protection in reverse supply connection.

Pin-Out

nr.	PAD	Description	TO-94 pin	Absolute max voltage with respect to			
				VREF (-)	VOUT (-)	GND (-)	VCC (-)
3a	VREF (+)	Reference/standby	1		4.6[d]/6.5[e]*	4.6[d]/6.5[e]	0.3
3b	VOUT (+)	Analog output	2	4.6[d]/6.5[e]		4.6[d]/6.5[e]	0.3
3c	GND (+)	Ground	3	0.3	0.3		0.3
3d	VCC (+)	Supply	4	4.6[d]/6.5[e]	4.6[d]/6.5[e]	4.6[d]/6.5[e]	

*=supply with device pins reversed (4↔1, 3↔2)

This table displays the absolute maximum voltage of the pads listed in columns (indicated by sign (+)), with respect to the other pads listed in the top line (indicated by sign (-)).

a 3-pin package (device MH485IVL).

b 4-pin package with VREF input/output pin (device MH486IVK).

c 4-pin package with STANDBY input pin (device MH487 IVK).

d 3.3V device

e 5V device

f 2.5V and VCC/10 voltage references are only supported with the 5V supplied devices.

Operation

User-programmable parameters

Parameter		Min	Typ	Max	Unit
Sensitivity	Symmetric range	9		250	V/T
	Asymmetric range	18		250	V/T
Sensitivity polarity		positive or negative			
Sensitivity TC		-250, 0, 250, 500, 750, 1000			ppm/°C
Reference voltage		internal or external			
VREF pin function		Vref (MH486) or standby (MH487)			
Internal reference voltage values		0.5, 1.65, 2.5[f], VCC/2, VCC/10[f]			V

Operating conditions

PARAMETER	Test Conditions	Specification			unit
		Min	Typ	Max	
Storage temperature		-40		125	°C
Operating temperature	TJ < 125°C	-40		115	°C
Supply voltage	B-field sensing	3[d]/4.5[e]	3.3[d]/5[e]	3.6[d]/5.5[d]	V
Supply current	V_{CC} = 5.0 V, R_L=10 kΩ	10	13	15	mA
Standby voltage	High impedance pin		Internally defined		V
Active voltage	Pull-down by <1kΩ			0.1-VCC	V
VOUT pin load resistance		2			kΩ
VOUT pin load capacitance	Fast response			6	nF
	Stable			100	
VREF pin load resisitance		200			kΩ
VREF pin load capacitance				60	nF

Qualification tests

Devices are qualified according to the following standards under specified conditions:

Test	Standard	Conditions
HBM ESD	JESD22-A114	4KV
Latch-up	JESD78	±100mA
HTSL	JESD22-A103	1000h，125℃
HTOL	JESD22-A108	1000h，125℃
THB	JESD22-A110	1000h，85%/85℃
TC	JESD22-A104	700cycles，-40℃/125℃
ELFR	JESD22-A108 JESD47	67h，125℃

Parametric specification

Parameters valid for a sample under operating conditions and after a single qualification test specified above, with supply voltage Vcc=5 V, unless specified otherwise under Test conditions.

Parameter	Test conditions	Min	Typ	Max	Unit
Supply current	RL ≥ 10kΩ		13	18	mA
	standby		8	16	µA
Reference voltage input current	External VREF mode		5.3	10.5	µA
Sensitivity change over lifetime	S = 125 V/T, Ta = 25 °C	-3		3	%
B-step propagation time	90% of B to 90 % of output voltage		3		µs
Signal bandwidth		120	170		kHz
Output voltage overshoot	CL = 6 nF	1	1	5	%
RMS output voltage noise	200 Hz-300 kHz				mV_{RMS}
	S=9 V/T		1.5		
	S=125 V/T		7.0		
Non-linearity	at 10% or 90% of input range wrt LSE, RL≥10 kΩ	-0.25		0.25	%
Reference voltage out	Ta = 25 °C, after trimming.	0.496	0.5	0.504	V
		1.646	1.65	1.654	V
		2.496	2.5	2.504	V
		VCC/2 -4m	VCC/2	VCC/2 +4m	V
		VCC/10 -4m	VCC/10	VCC/10 +4m	V
Reference voltage in		0.5		VCC/2	V
Quiescent output voltage	B = 0 µT		Vref		V
Output voltage offset (Vout-Vref)	B = 0 µT, S=125 V/T	-6		6	mV
Output voltage offset shift over lifetime		-3		3	mV
Offset voltage TC	B = 0 µT, S=125 V/T, excluding Vref offset	-0.120		0.120	mV/°C
Minimum output voltage	RL=10 kΩ			0.15	V
Maximum output voltage	RL=10 kΩ	VCC-0.15			V
VOUT pin sink current	VOUT shorted to VCC	-40		-20	mA
VOUT pin source current	VOUT shorted to VSS	28		60	mA

Application diagram

The application diagram of Figure 5 to Figure 7 show the chip connection for corresponding operation.

The analog signal pins VOUT and VREF are referred to GND; therefore, loads or sources on these pins must also refer to GND.

It is recommended to place a ceramic decoupling capacitor of 47nF or more as close as possible to the IC. This is a minimal countermeasure for preventing EMC issues. If VREF is used, a decoupling capacitor may be added there too for optimum EMI performance.

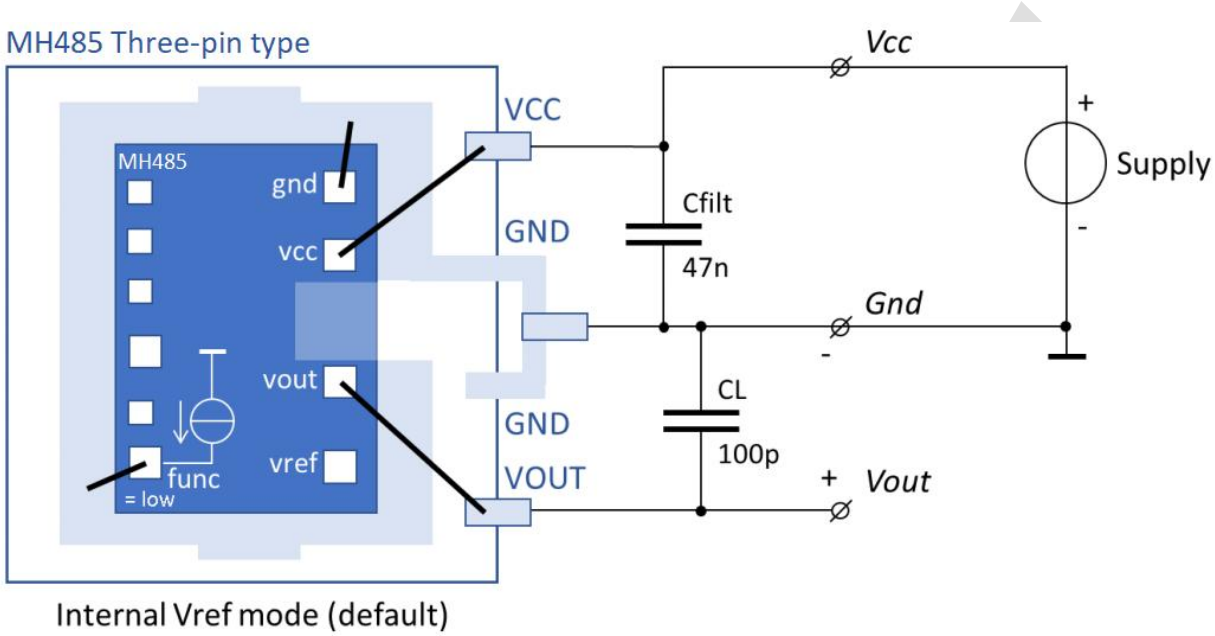


Figure 4: Basic application diagram – Internal VREF mode three-pins device MH485EVL.

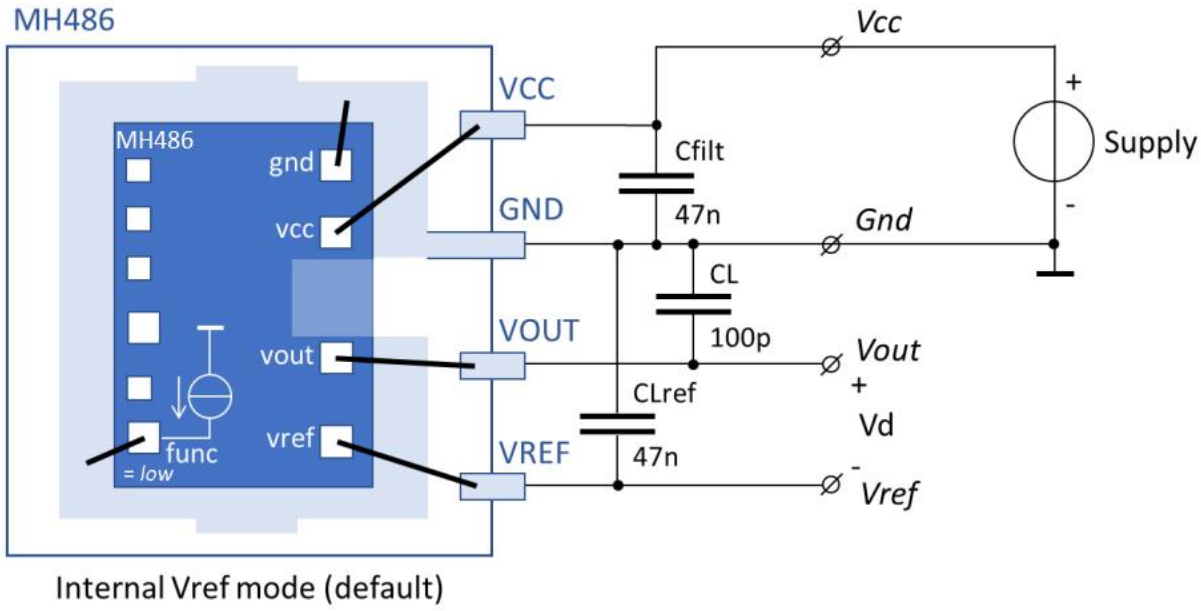


Figure 5: Basic application diagram – Internal VREF mode device MH486.

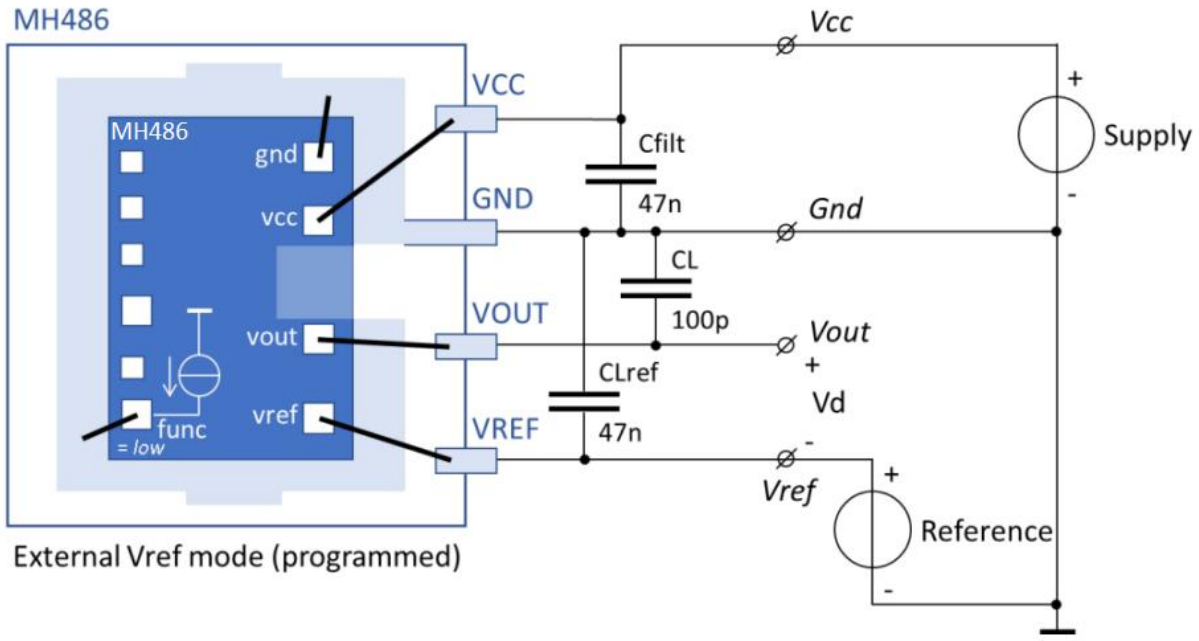


Figure 6: Basic application diagram – External VREF mode device MH486.

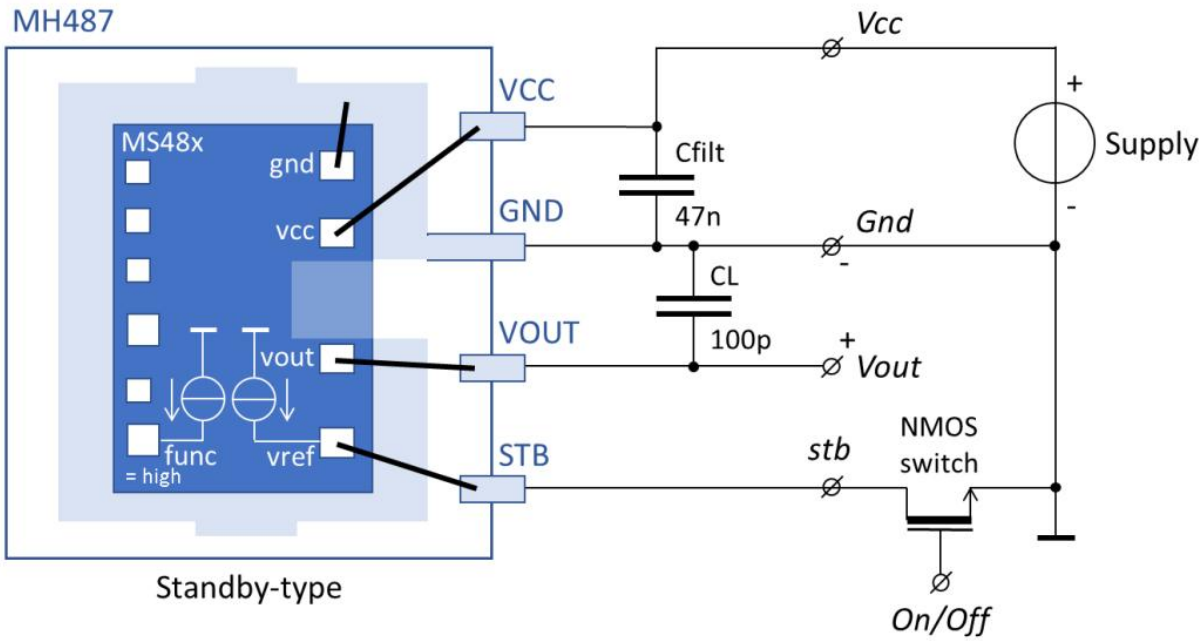
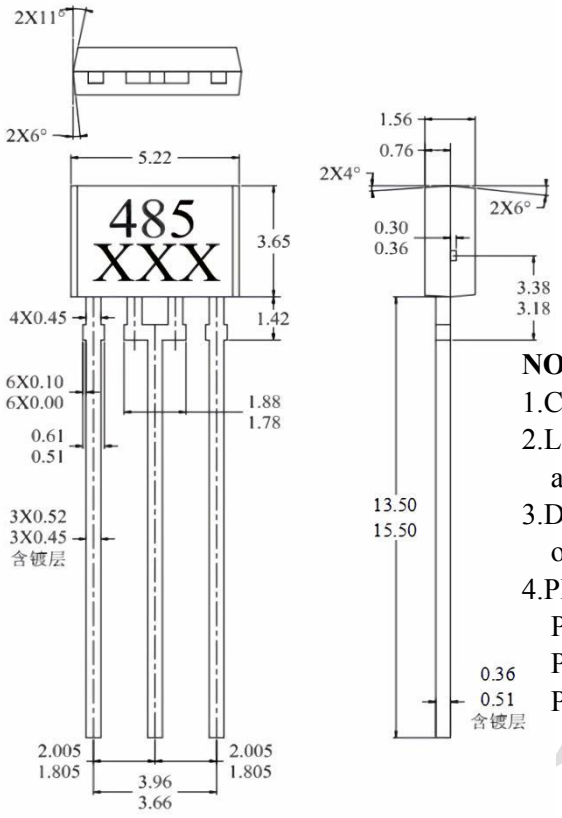


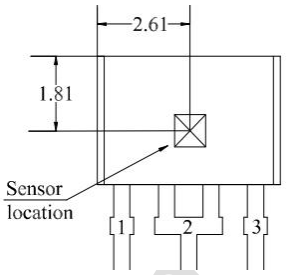
Figure 7: Basic application diagram – Standby type device MH487.

Sensor Location, Package Dimension and Marking

VL Package (To-94-3pin)



Hall Chip location

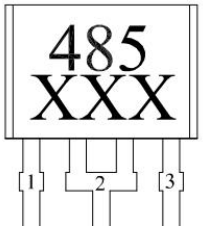


NOTES:

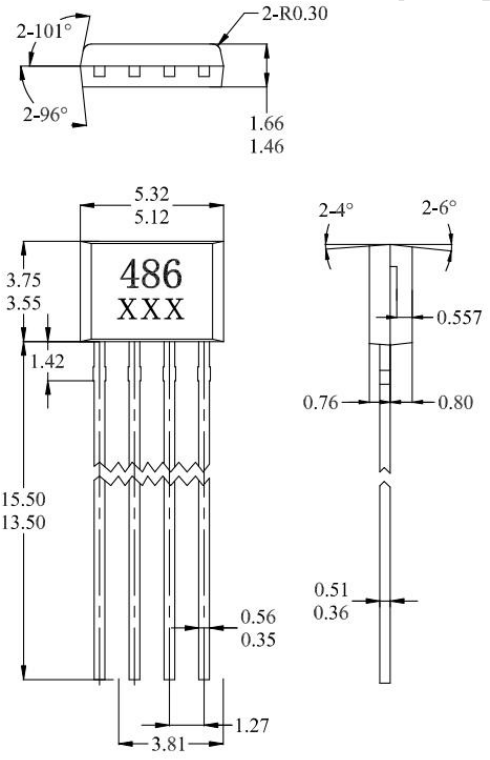
1.Controlling dimension: mm
2.Leads must be free of flash and plating voids
3.Do not bend leads within 1 mm of lead to package interface.
4.PINOUT:

Pin 1	VOUT
Pin 2	GND
Pin 3	VCC

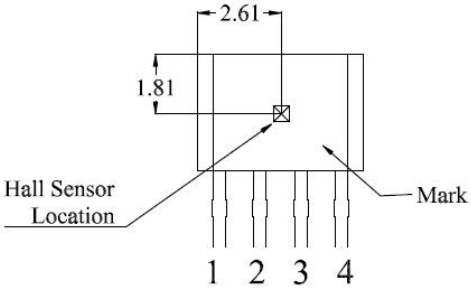
Output Pin Assignment



VK Package (To-94-4pin)



Hall Chip location

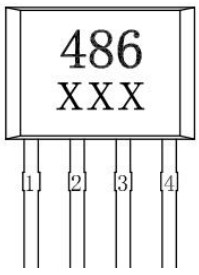


NOTES:

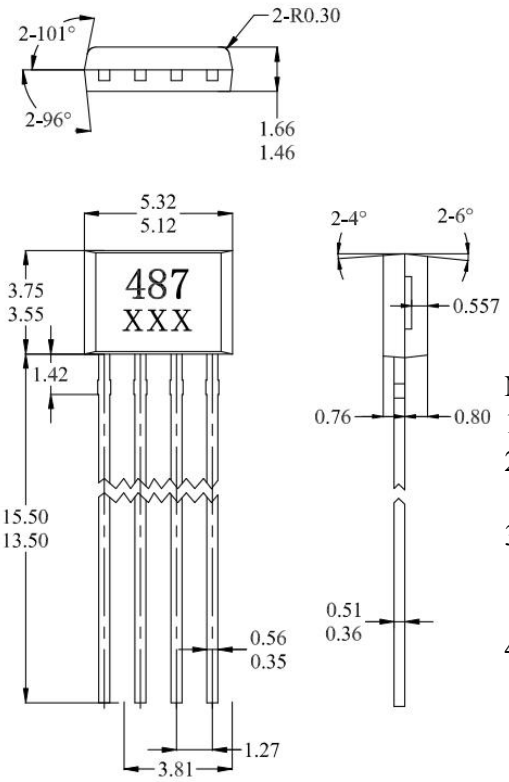
1.Controlling dimension: mm
2.Leads must be free of flash and plating voids
3.Do not bend leads within 1 mm of lead to package interface.
4.PINOUT:

Pin 1	VREF
Pin 2	VOUT
Pin 3	GND
Pin 4	VCC

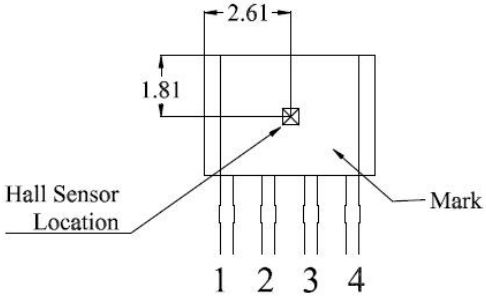
Output Pin Assignment



VK Package (To-94-4pin)



Hall Chip location



NOTES:

1.Controlling dimension: mm

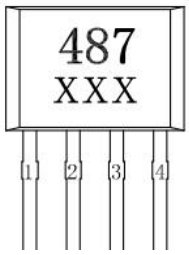
2.Leads must be free of flash and plating voids

3.Do not bend leads within 1 mm of lead to package interface.

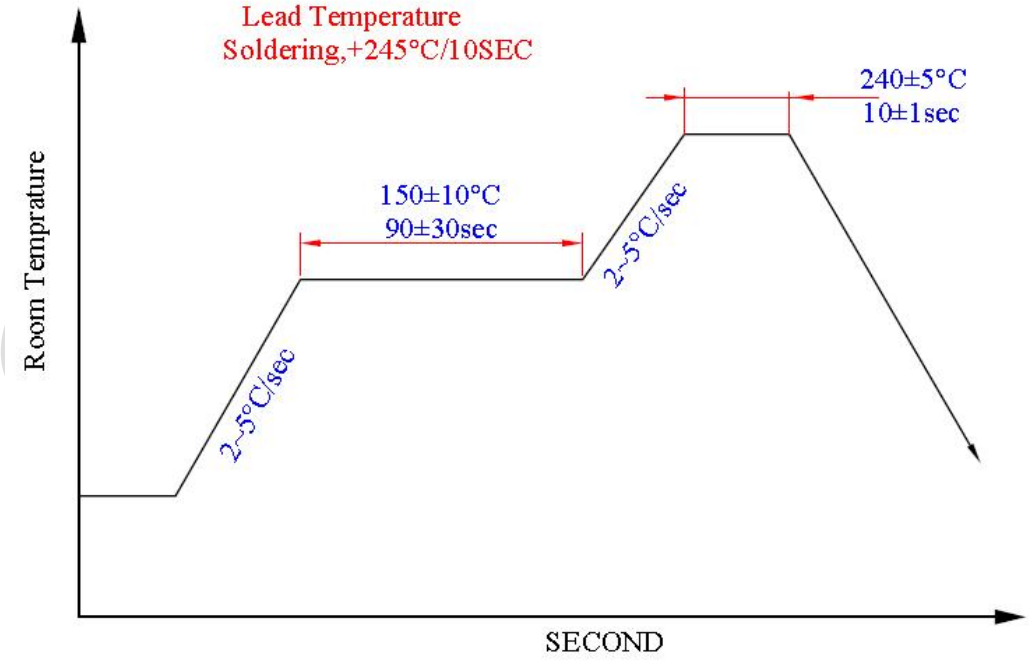
4.PINOUT:

Pin 1	STB
Pin 2	VOUT
Pin 3	GND
Pin 4	VCC

Output Pin Assignment



IR reflow curve



VK/VL Soldering Condition

Packing specification:

TO-94-4PIN	Weight	TO-94-3PIN	Weight
1000pcs/Bag	0.16kg	1000pcs/Bag	0.149kg
10 Bags/Box	1.82kg	10 Bags/Box	1.64kg
10 Boxes/Carton	18.98kg	10 Boxes/Carton	17.18kg
5 Boxes/Carton	9.63kg	5 Boxes/Carton	8.73kg
4 Boxes/Carton	7.79kg	4 Boxes/Carton	7.07kg

VK/VL Package Inner box label ：Size: 5cm*8cm

VK/VL Carton label ：Size: 6 cm * 9cm

Combine:

When combine lot, one bag could have two D/C and no more than two DC. One carton could have two devices, no more than two;