MH233 Hall-effect sensor is a temperature stable, stress-resistant, Low Tolerance of Sensitivity Ultra-power switch. Superior high-temperature performance is made possible through a dynamic offset cancellation that utilizes chopper-stabilization. This method reduces the offset voltage normally caused by device over molding, temperature dependencies, and thermal stress.

MH233 is special made for low operation voltage, 2.7V, to active the chip which is includes the following on a single silicon chip: voltage regulator, Hall voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, CMOS output driver. Advanced CMOS wafer fabrication processing is used to take advantage of low-voltage requirements, component matching, very low input-offset errors, and small component geometries. This device can be operated on not only unipolar S or N, but omni-polar magnetic field.

The package type is in a Halogen Free version has been verified by third party Lab.

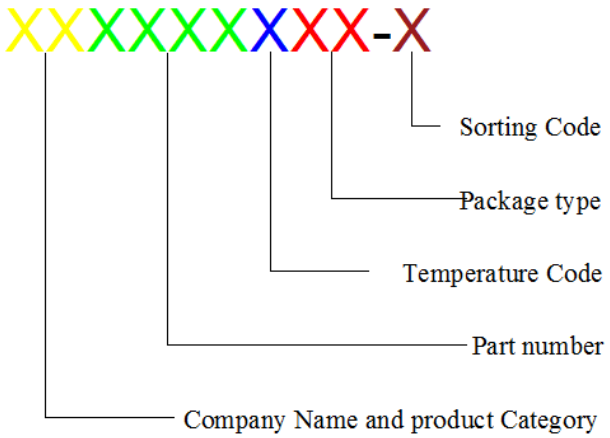
Features and Benefits

- CMOS Hall IC Technology
- Strong RF noise protection
- 2.7 to 5.5V for battery-powered applications
- Omni polar, output switches with absolute value of North or South pole from magnet
- Operation down to 2.7V， Micro power consumption
- High Sensitivity for reed switch replacement applications
- Low sensitivity drift in crossing of Temp. rang
- Multi Small Size option
- Ultra low power consumption at 1.6uA (Avg)
- High ESD Protection, HBM > ±4KV(min)
- Operation with South Pole (OUT1) or North Pole (OUT2)
- Totem-pole output
- RoHS compliant 2011/65/EU and Halogen Free

Applications

- Solid state switch
- Handheld wireless Handset Awake Switch(Flip Cell/PHS Phone/Note Book/Flip Video Set)
- Magnet proximity sensor for reed switch replacement in low duty cycle applications
- Water Meter
- PDA
- Tab PC
- Security
- Smart meter
- 3C
- TWS

Ordering Information



Company Name and Product Category

MH:MST Hall Effect/MP:MST Power MOSFET

Part number

181,182,183,184,185,248,249,276,477,381,381F,381R,382…..

If part # is just 3 digits, the forth digit will be omitted.

Temperature range

E: 85 ℃, I: 105 ℃, K: 125 ℃, L: 150 ℃

Package type

UA:TO-92S,VK:TO-92S(4pin),VF:TO-92S(5pin),SO:SOT-23,

SQ:QFN-3,ST:TSOT-23,SN:SOT-553,SF:SOT-89(5pin)

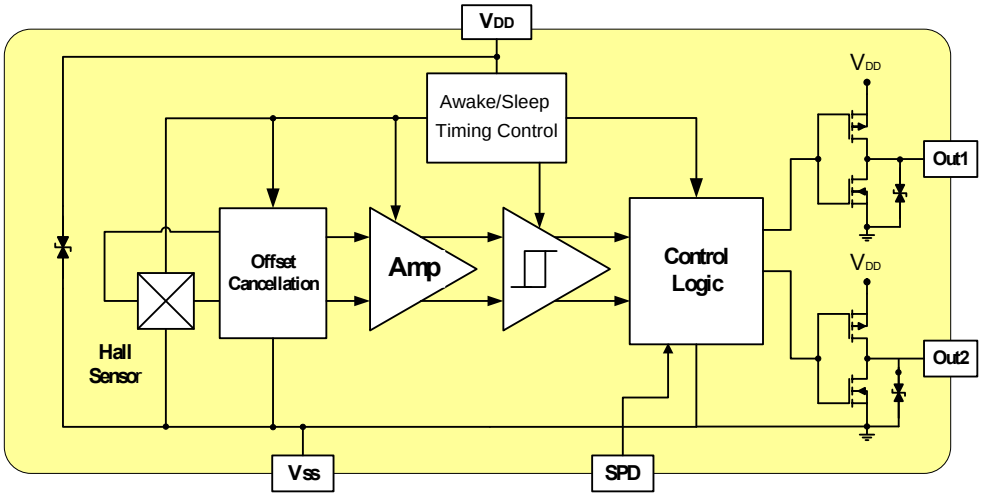
Sorting

α,β,Blank…..

Part No.	**Temperature Suffix**	**Package Type**
MH233NEUA	E (-40℃ to + 85℃)	UA (TO-92S)
MH233SEUA	E (-40℃ to + 85℃)	UA (TO-92S)
MH233NEST	E (-40℃ to + 85℃)	ST (TSOT-23)
MH233SEST	E (-40℃ to + 85℃)	ST (TSOT-23)
MH233ESD	E(-40℃ to +85℃)	SD (DFN2*2-6L)
MH233ESS	E (-40℃ to + 85℃)	SS (QFN1x1-4L)

Custom sensitivity selection is available by MST sorting technology

Functional Diagram



***Note**: Static sensitive device; please observe ESD precautions. Reverse V_{DD} protection is not included. For reverse voltage protection, a 100Ω resistor in series with V_{DD} is recommended.*

MH233, HBM > ±4KV which is verified by third party lab.

Absolute Maximum Ratings *At(Ta=25℃)*

Characteristics		Values	Unit
Supply voltage, (V_{DD})		6.0	V
Output Voltage, (*Vout*)		6.0	V
Reverse Voltage, (V_{DD} / V_{OUT})		-0.3	V
Magnetic flux density		Unlimited	Gauss
Output current, (I_{OUT})		5	mA
Operating temperature range, (*Ta*)		-40 to +85	℃
Storage temperature range, (*Ts*)		-65 to +150	℃
Maximum Junction Temp, (*Tj*)		150	℃
Thermal Resistance	(θ_{JA}) UA/ST/SS/SD	206/543/300/160	℃/A
	(θ_{JC}) UA/ST/SS/SD	148/410/52/35	℃/A
Package Power Dissipation, (P_D) UA/ST/SS/SD		606/230/416/780	mW

Note: *Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.*

Electrical Specifications

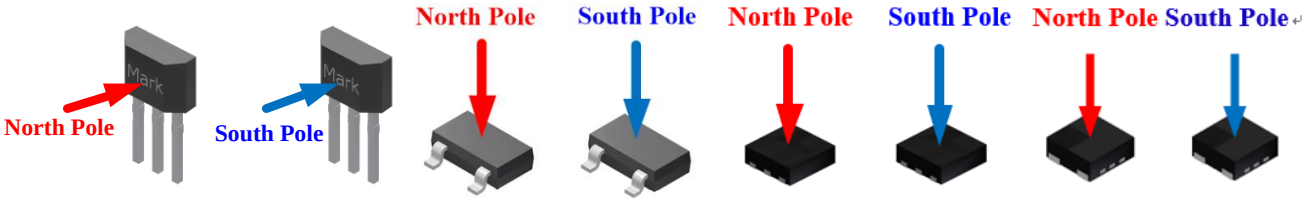
DC Operating Parameters ：Ta=25℃, V_{DD}=3.0V

Parameters	Test Conditions	Min	Typ	Max	Units
Supply Voltage (V_{DD})	Operating	2.7		5.5	V
Supply Current (I_{DD})	Awake State		2.0		mA
	Sleep State		1.0		μA
	Average (SPD=Hi)		1.6/(135)		μA
Output High Voltage (V_{OH})	I_{OUT}=1.0mA (Source)	VDD-0.2			V
Output Low Voltage (V_{OL})	I_{OUT}=1.0mA (Sink)			0.2	V
Awake mode time, (*Taw*)	Operating		20	40	uS
Sleep mode time, (*TSL*)	Operating (SPD=Hi)		80(0.16)	150(0.32)	mS
Duty Cycle, (*D,C*)	(SPD=Hi)		0.025/(12.5)		%
Power-On Time, (T_{PO})			16	32	nS
Output Switch Time, (T_{SW})	Operating (SPD=Hi)		80(0.2)	160(0.4)	mS
Output Switch Frequency, (F_{SW})	Operating (SPD=Hi)	15(6.5k)			Hz
Electro-Static Discharge	HBM	4			KV
Operate Point, $B_{OP}S$ (Output S)	$B>B_{OP}S$	50		90	Gauss
Release Point, $B_{RP}S$ (Output S)	$B<B_{RP}S$	40		80	Gauss
Operate Point, $B_{OP}N$ (Output N)	$B>\|B_{OP}N\|$	-90		-50	Gauss
Release Point, $B_{RP}N$ (Output N)	$B<\|B_{RP}N\|$	-80		-40	Gauss
Hysteresis, (BHYS)	$\|B_{OP}X - B_{RP}X\|$		10		Gauss

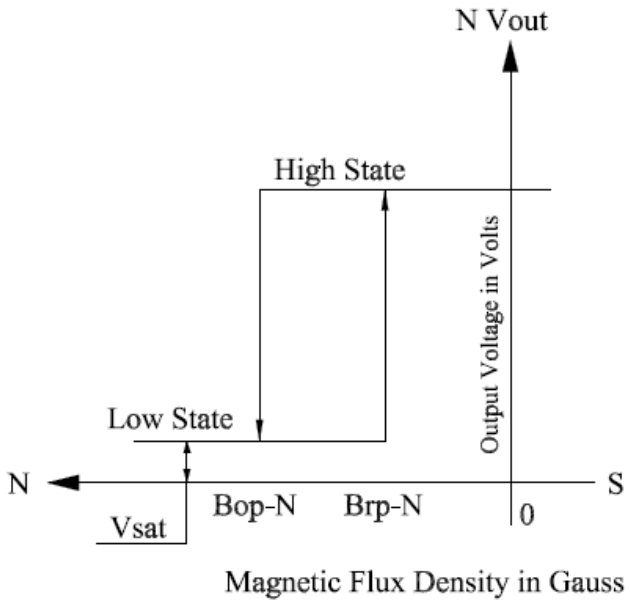
MH233NEUA/SEUA/NEST/SEST/ESS/ESD Output Behavior versus Magnetic Polar

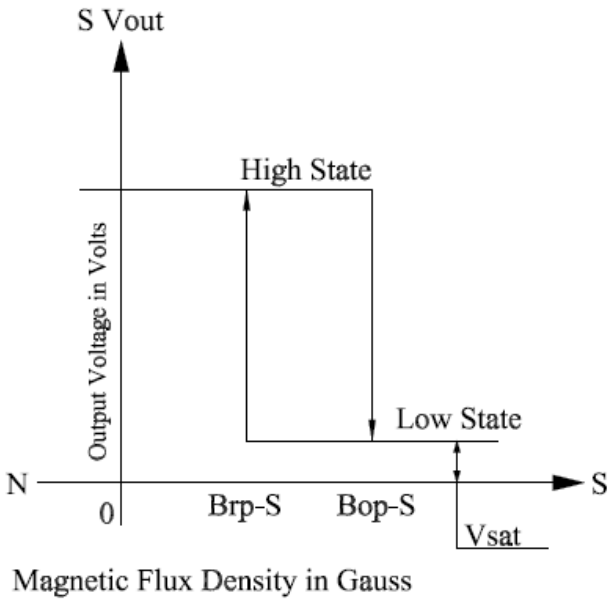
DC Operating Parameters： Ta = -40 to 85℃, V_{DD} =2.7V to 5.5V

Parameter	*Test condition*	*S vout*	*Test condition*	*N Vout*
South pole	B > $B_{OP}S$	Low	--	High
Null or weak magnetic field	B=0 or B < $B_{RP}S$	High	B=0 or B <|$B_{RP}N$|	High
North pole	--	High	B >|$B_{OP}N$|	Low

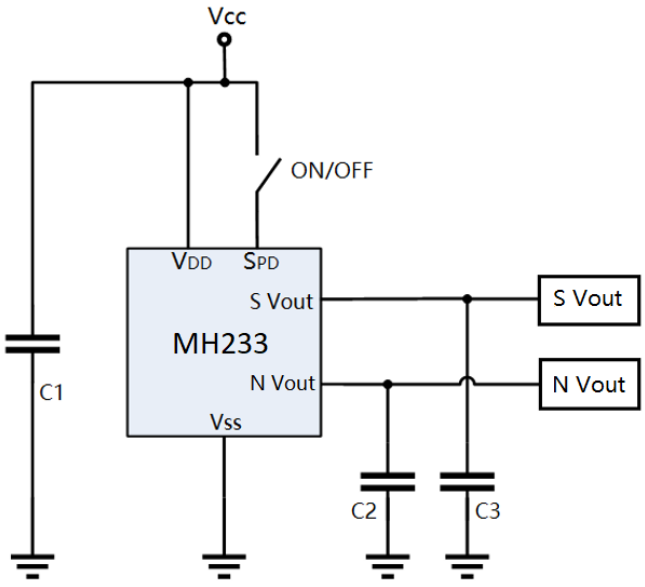


UA Package *ST Package* *SD Package* *SS Package*





Typical application circuit

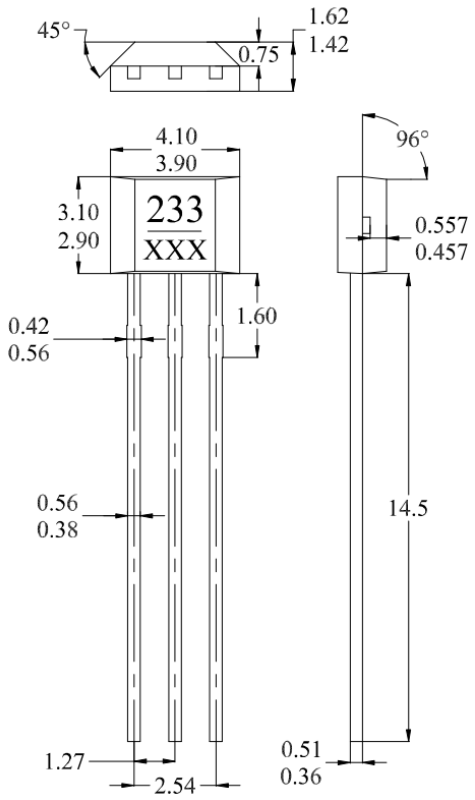


C1：10nF

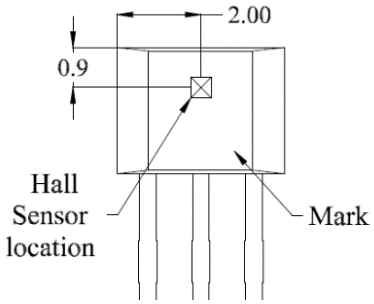
C2：100pF

Sensor Location, package dimension and marking

MH233SEUA Package



Hall Chip location

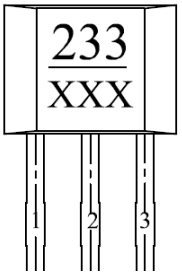


NOTES:

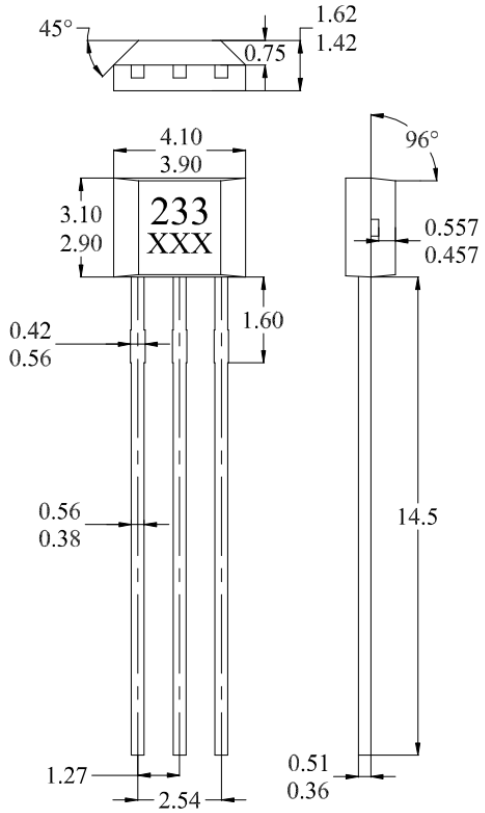
1. Controlling dimension: mm
2. Leads must be free of flash and plating voids
3. Do not bend leads within 1 mm of lead to package interface.
4. PINOUT:
   Pin 1 VCC
   Pin 2 GND
   Pin 3 Output
5. XXX； 1st X=Year； 2nd and 3rd XX=Week

Output Pin Assignment

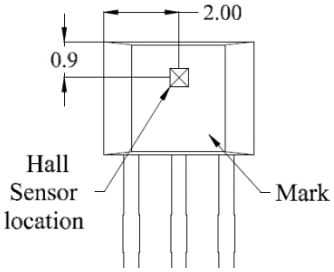
(Top view)



MH233NEUA Package



Hall Chip location

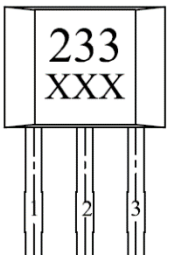


NOTES:

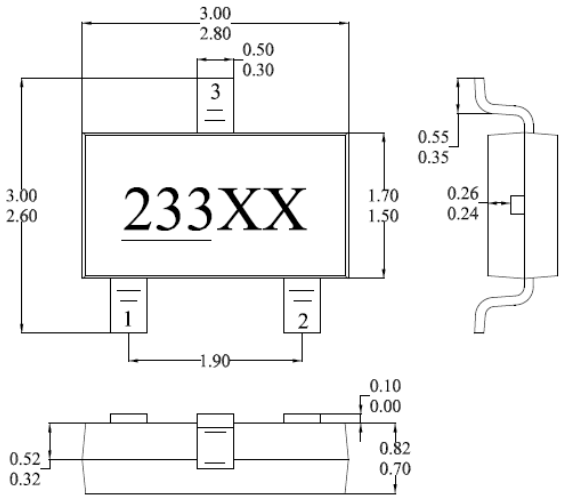
1. Controlling dimension: mm
2. Leads must be free of flash and plating voids
3. Do not bend leads within 1 mm of lead to package interface.
4. PINOUT:
   Pin 1 VCC
   Pin 2 GND
   Pin 3 Output
5. XXX； 1st X=Year；
   2nd and 3rd XX=Week

Output Pin Assignment

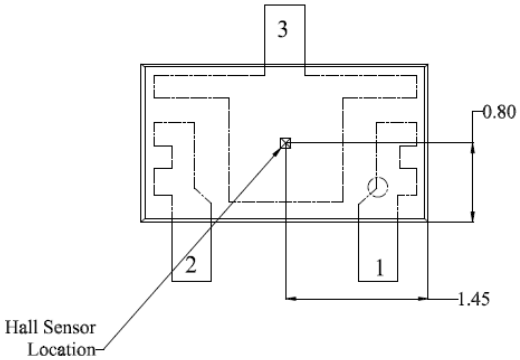
(Top view)



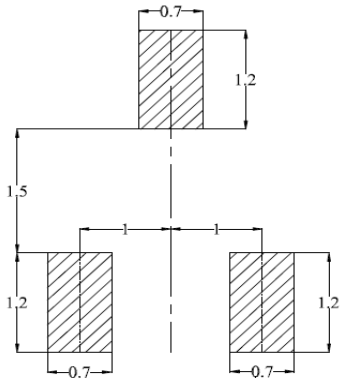
MH233SEST Package
(Top View)



Hall Plate Chip Location
(Bottom view)



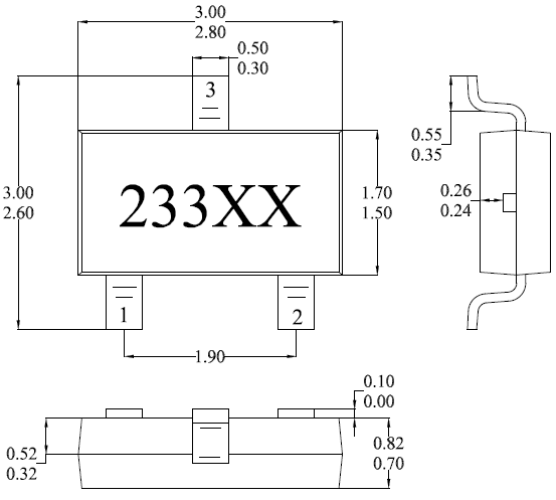
(For reference only) Land Pattern



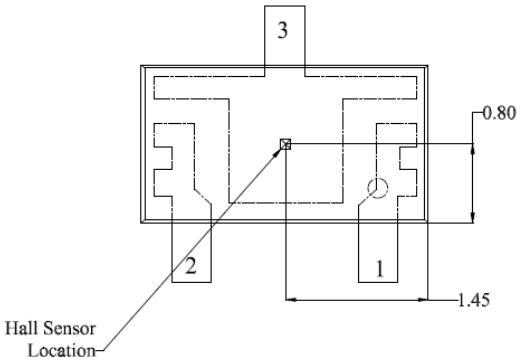
NOTES:

1. PINOUT (See Top View at left :)
   Pin 1 V_{DD}
   Pin 2 Output
   Pin 3 GND
2. Controlling dimension: mm
3. Lead thickness after solder plating will be 0.254mm maximum
4. XX: Date Code, Refer to DC table

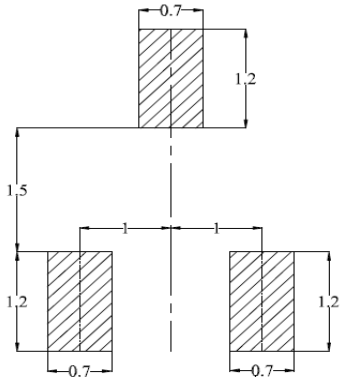
MH233NEST Package
(Top View)



Hall Plate Chip Location
(Bottom view)



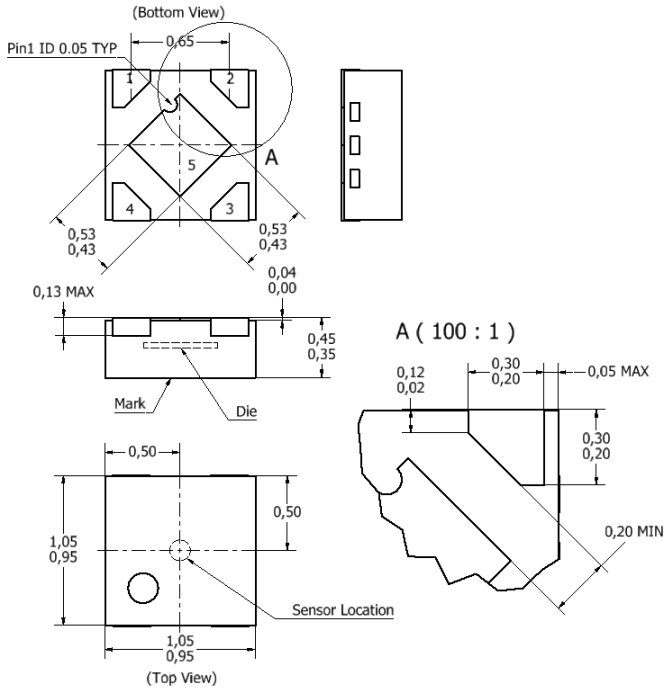
(For reference only) Land Pattern



NOTES:

1. PINOUT (See Top View at left :)
   Pin 1 V_{DD}
   Pin 2 Output
   Pin 3 GND
2. Controlling dimension: mm
3. Lead thickness after solder plating will be 0.254mm maximum
4. XX: Date Code, Refer to DC table

SS Package (DFN 1.0*1.0-4L)



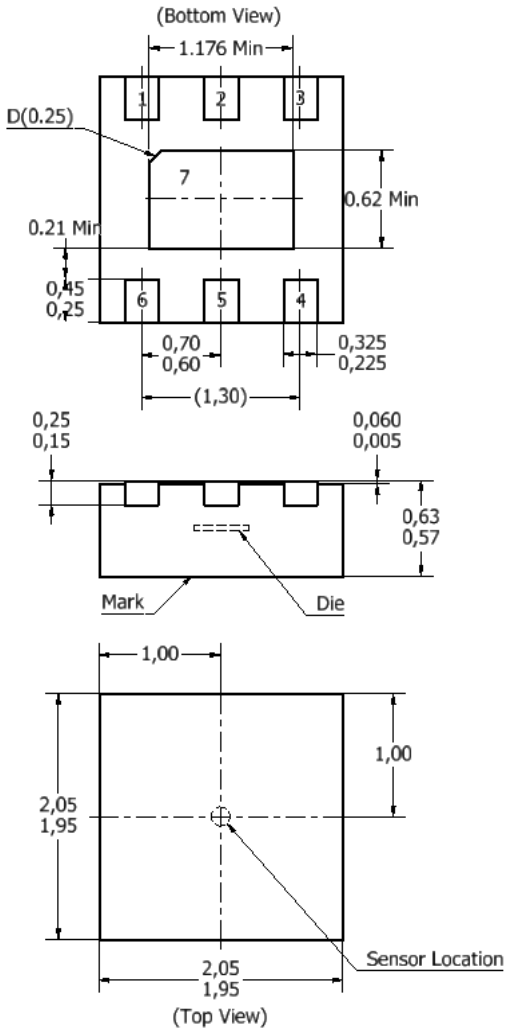
NOTES:

Controlling dimension: mm

1. Leads must be free of flash and plating voids
2. Lead thickness after solder plating will be 0.254mm maximum
3. PINOUT:

Pin No.	Pin Name	Function
1	V_{DD}	Power Supply
2	V_{SS}	Ground
3	S V_{OUT}	Output1
4	N V_{OUT}	Output2
5	PAD	NC

SD Package (DFN2*2-6L)



NOTES:

1. Controlling dimension: mm
2. Leads must be free of flash and plating voids
3. Lead thickness after solder plating will be 0.254mm maximum
4. PINOUT:

Pin No.	Pin Name	Function
1	V_{DD}	Power Supply
2	N V_{OUT}	Output2
3	S V_{OUT}	Output1
4	N.C	N.C
5	V_{SS}	Ground
6	SPD	Set pin
7	PAD	Ground

5. （For reference only）Land pattern